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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,474	12/03/2003	Hidetoshi Narahara	60188-721	5418

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EXAMINER	
PATEL, SHAMBHAVI K	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 09/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/725,474	NARAHARA, HIDETOSHI	
	Examiner	Art Unit	
	Shambhavi Patel	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *10 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-7 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-7 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-7 are pending.

Response to Arguments

1. **Regarding the rejection of Independent Claim 1 under 35 USC § 102(e):**

Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

2. **Regarding the rejection of Dependent Claims 2-4 and 7 under 35 USC § 102(b):**

Applicant's arguments with respect to claims 2-4 and 7 have been considered but are moot in view of the new ground(s) of rejection

3. **Regarding the rejection of Independent Claims 5 and 6 under 35 USC § 102:**

Applicant's arguments filed 10 July 2006 have been fully considered but they are not persuasive.

The Applicant submits that McNamara does not disclose 'analyzing correspondence information that represents correspondence between combination of the signals used in hardware emulation process which correspond to input signals to the description block and executed rows' because analyzing the correspondence information representing the correspondence between the signals and executed rows in the claims is different from constructing vectors proving whether blocks are correct. The Applicant is directed to **figure 5A** of the prior art. *Coverage information* for the design *(including input variables)* is collected. The *coverage information is then analyzed* to determine which areas have not been covered, and test vectors for those areas are then generated. The Applicant is directed to **figure 5B** of the prior art. After the test vectors are generated, the design is simulated under

the new vectors. *Coverage data is then regenerated, and reanalyzed* to determine if any area remains untested; if so, the process is repeated.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. **Claims 1 is rejected under 35 U.S.C. 112, second paragraph**, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). The preamble states "A simulation method for executing description rows of each description block describing functions of a semiconductor device to simulate the operation of the semiconductor device, each description block including first to nth description rows..." but the body of the claim does not depend on this.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. **Claims 1-7 are rejected under 35 U.S.C. 101** because the claimed invention is directed to non-statutory subject matter. The Examiner asserts that the current state of the claim language is such that a reasonable interpretation of the claims would not result in any useful, concrete or tangible product. Generating an execution history (claim 1) or a coverage result (claims 5 and 6) does not produce a tangible result. The results are not outputted to a file or displayed, and the claims fail to use or make available for use the result of the determination to enable its functionality and usefulness to be realized. All other claims are rejected by virtue of their dependency.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claim 1 is rejected under 35 U.S.C. 102(e)** as being clearly anticipated by **Roediger (US Patent No. 6,938,249).**

Regarding claim 1:

Roediger is directed to a simulation method for executing description rows of each description block describing functions of a semiconductor device to simulate the operation of the semiconductor device, each description block including first to nth description rows for each description block, comprising the steps of:

a. executing a description row for a description block during a simulation time **(column 7 lines 62-63).** The code is first instrumented, and the run in order to obtain profile data.

b. generating an executed row-history for the description block indicating an executed row in the simulation time **(column 4 lines 19-22).** The instrumented code keeps track of whether or not a particular branch *(i.e. row)* is taken.

c. every time the first row in the description block is executed during that simulation time **(column 8 lines 59-61)**, deleting the executed-row history previously generated in the simulation time and generating a new executed-row history for the description block to generate the coverage result **(column 7 lines 56-57).** Every time a loop is entered during execution *(i.e. the first row in the description block is entered),* a counter is incremented *(i.e. the old history is deleted and replaced with a new one).*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. **Claims 5 and 6 are rejected under 35 U.S.C. 102(b)** as being anticipated by **McNamara (US Patent No. 6,141,630).**

Regarding claim 5:

McNamara discloses an emulation method, comprising the steps of:

i. extracting, for each description block, signals used in a hardware emulation process which correspond to input signals to the description block **(column 3 lines 62-64).**

ii. analyzing correspondence information that represents correspondence between combinations of the signals used in hardware emulation process which correspond to input signals to the description block and executed rows **(column 4 lines 28-26; figures 5A and 5B)**. McNamara discloses a test generator that creates a test vector by determining which block, transition, or path has not been verified. The generator determines what variables need to be set or what conditions need to occur so that the simulated design transitions to an untested element from the current active block.

iii. tracing the signals which correspond to input signals to each description block and analyzing executed rows according correspondence between the input signals to the description block and the executed rows and a result of the tracing of the signals used in the hardware emulation process which correspond to the input signals to the description block **(column 5 lines 11-15)**. During the iterative test generator uses the data in the coverage database to determine whether the simulated design is correct for all inputs. The generator correlates the test vectors (or inputs) sent to the simulated design with the results from the model to determine which of the design blocks operate incorrectly **(column 5 lines 48-54).**

Regarding claim 6:

McNamara discloses an emulation method, comprising the steps of:

i. extracting, for each logic cone, signals used in a hardware emulation process which correspond to input signals to the logic cone **(column 3 lines 62-64).** The design block disclosed by McNamara is analogous to the logic cones in the claim.

ii. analyzing correspondence information that represents correspondence between combinations of the signals used in the hardware emulation process which correspond to input signals to the logic cone and executed rows **(column 4 lines 28-26; figures 5A and 5B).** McNamara discloses a test generator that creates a test vector by determining which block, transition, or path has not been verified. The generator determines what variables need to be set or what conditions need to occur so that the simulated design transitions to an untested element from the current active block.

iii. in an emulation execution process, tracing the input signals to each logic cone and analyzing executed rows according to correspondence between the input signals to the logic cone and the executed rows and a result of the tracing of the signals used in the hardware emulation process which correspond to the input signals to the logic cone **(column 5 lines 11-15).** During the iterative test generator uses the data in the coverage database to determine whether the simulated design is correct for all inputs. The generator correlates the test vectors (or inputs) sent to the simulated design with the results from the model to determine which of the design blocks operate incorrectly **(column 5 lines 48-54).**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. **Claim(s) 2-4 and 7 are rejected under 35 U.S.C. 103(a)** as being unpatentable over **Roediger (US Patent No. 6,938,249) in view of McNamara (US Patent No. 6,141,630).**

Regarding claim 2:

Roediger does not explicitly disclose the elements of this claim.

McNamara teaches a simulation method, comprising the steps of

i. analyzing, for each description block, correspondence information that represents correspondence between combinations of input signals to the description block and executed rows **(McNamara: column 4 lines 28-26; figures 5A and 5B)**. McNamara discloses a test generator that creates a test vector by determining which block, transition, or path has not been verified. The generator determines what variables need to be set or

what conditions need to occur so that the simulated design transitions to an untested element from the current active block.

ii. in a simulation execution process, tracing input signals to each description block and analyzing the executed rows according to an analysis result of the correspondence information that represents the correspondence between combinations of input signals to the description block and executed rows and a trace result of the input signals to the description block **(McNamara: column 5 lines 11-15)**. During the iterative test generator uses the data in the coverage database to determine whether the simulated design is correct for all inputs. The generator correlates the test vectors (or inputs) sent to the simulated design with the results from the model to determine which of the design blocks operate incorrectly **(McNamara: column 5 lines 48-54)**.

iii. the executed row history for the description block is generated based on the combination of the input signals and the executed row **(McNamara: column 5 lines 49-54)**.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Roediger and McNamara because the process taught by McNamara permits testing of basic blocks, transition arcs, and paths of interest within the simulated design using a quick, easy, comprehensive, and integrated process **(McNamara: column 2 lines 43-52)**.

Regarding claim 3:

Roediger does not explicitly disclose the elements of this claim.

McNamara teaches all of the limitations of the claim shown above in the rejection claim 2, further including obtaining the trace results every unit time. McNamara is directed to the method in claim 2 wherein all changes in the signals are tracked **(McNamara: column 6 lines 50-59)**. The test generator is able to directly target transition paths, and thus is able to determine if the input results in the correct

change in the signal **(McNamara: column 7 lines 16-36)**. At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Roediger and McNamara because the process taught by McNamara permits testing of basic blocks, transition arcs, and paths of interest within the simulated design using a quick, easy, comprehensive, and integrated process **(McNamara: column 2 lines 43-52).**

Regarding claim 4:

Roediger does not explicitly disclose the elements of this claim.

McNamara teaches all of the limitations of the claim shown above in the rejection claim 2, further including obtaining the trace results every cycle. McNamara is directed to the method of claim 2, wherein the model is cycle-accurate **(McNamara: column 5 lines 60-67; column 6 lines 1-7)**. The model receives test vectors from the test generator and matches cycle-for-cycle the output data from the simulated design. At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Roediger and McNamara because the process taught by McNamara permits testing of basic blocks, transition arcs, and paths of interest within the simulated design using a quick, easy, comprehensive, and integrated process **(McNamara: column 2 lines 43-52).**

Regarding claim 7:

Roediger does not explicitly disclose the elements of this claim.

McNamara teaches a simulation method, comprising the steps of:

i. analyzing, for each description block, input conditions for executing respective rows included in the description block **(McNamara: column 3 lines 62-64)**.

ii. analyzing correspondence information that represents correspondence between the input conditions and executed rows **(McNamara: column 4 lines 28-26).** McNamara discloses

a test generator that creates a test vector by determining which block, transition, or path has not been verified. The generator determines what variables need to be set or what conditions need to occur so that the simulated design transitions to an untested element from the current active block.

iii. in a simulation execution process, tracing input signals to each description block and analyzing executed rows based on the correspondence information that represents the correspondence between the input conditions and the executed rows and a tracing result of the input signal to the description block **(McNamara: column 5 lines 11-15)**. During the iterative test generator uses the data in the coverage database to determine whether the simulated design is correct for all inputs. The generator correlates the test vectors (or inputs) sent to the simulated design with the results from the model to determine which of the design blocks operate incorrectly **(column 5 lines 48-54).**

iv. the executed row history for the description block is generated based on the combination of the input signals and the executed row **(McNamara: column 5 lines 49-54)**.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Roediger and McNamara because the process taught by McNamara permits testing of basic blocks, transition arcs, and paths of interest within the simulated design using a quick, easy, comprehensive, and integrated process **(McNamara: column 2 lines 43-52).**

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shambhavi Patel whose telephone number is (571) 272-5877. The examiner can normally be reached on Monday-Friday, 8:00 am – 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-2279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SKP

KAMINI SHAH
SUPERVISORY PATENT EXAMINER